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EXAMINER	
BLAIR, KILE O	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/828,342	MAGRATH, ANTHONY J.	
	Examiner	Art Unit	
	Kile O. Blair	4114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9,11-27,29,30 and 32-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,11-27,29,30 and 32-39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *01/07/2005, 12/08/2004*.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

DETAILED ACTION

1. This action is in response to the Preliminary Amendment filed on 9/28/2005, claims10, 28, and 31 have been canceled, claims 1-9, 11-27, 29-30, and 32-36 and the newly added claims 37-39 are pending.

Claim Objections

2. Claim 9 is objected to under 37 CFR 1.75(b) as being improper because it is identical to claim 3. See MPEP § 608.01(i).

Claim 15 is objected to because "a time dependent characteristics" is incorrect grammar.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 26, 32, and 33 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 26, the claim involves improper grammar (indicative signal scaled signal) that renders the claim indefinite.

Regarding claim 32, the claim is worded in an indefinite manner and involves incorrect grammar.

Regarding claim 33, "carrier" is indefinite because it can have no meaning and one of ordinary skill in the art would not know what meaning is intended.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claims 1-9, 11-27, 29, 30 and 32-39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lynn (US Pat. No. 4,928,307) in view of Walker et al. (US Pat. No. 4,809,274).

Regarding claim 1, Lynn teaches a gain determining stage for determining gain signal to be applied to amplify a digital audio signal (voice signal compression system including variable gain amplifier for amplifying the voice input signal; Lynn, Col. 2, lines 39-43), the stage comprising: an input for receiving a parameter of said digital audio

signal (where the parameter is the comparator output pulse indicating when the peaks of the input signal received through input 12 (Fig. 2) exceed the threshold; Lynn, Col. 2, line 54-56); an adjuster for adjusting said parameter dependent on a received volume control signal (where the adjuster is the variable gain amplifier which is controlled by control voltage; Lynn, Col. 2, lines 49-52); and a gain selector for applying a variable gain function to said volume control signal in order to generate a gain signal for applying to the digital audio signal (where the gain selector is the variable gain amplifier which is controlled by control voltage; Lynn, Col. 2, lines 49-52); and wherein said variable gain function is dependent on said adjusted parameter (control voltage which is produced by attack/delay timing generator dependent on the peaks of the input signal; Lynn, Col. 2, lines 49-56). Although Lynn does not explicitly teach the feature of using a digital audio signal as required, it would have been obvious for one of ordinary skill in the art to do so with the motivation of conserving transmission bandwidth as taught by Walker et al (Col. 1, lines 15-16).

Regarding claim 2, Lynn teaches a gain determining stage according to claim 1 wherein the received volume control signal is input to a processor before being passed to the adjuster (the control voltage passes through the threshold/reset timer which processes the signal by switching it to a lower level through logarithmic conversion and then control voltage passes to the variable gain amplifier; Lynn, Col. 2, lines 58-62).

Regarding claim 3, Lynn teaches a gain determining stage according to claim 2 wherein the processor comprises a log converter and/or a scaling means (the threshold/

reset timer scales the signal down 10 decibels when the signal is continuous, Lynn, Col. 4, lines 37-41).

Regarding claim 4, Lynn teaches a gain determining stage according to claim 1 comprising a log converter for log converting the received parameter and an adder for adding the volume control signal to the log parameter (the compression threshold of the comparator is converted down by 10dB logarithmically {Lynn, Col. 4, lines 37-41} and then the comparator output is added into the volume control signal; Lynn, Col. 4, lines 53-56). Although Lynn does not explicitly teach that the adder is located in the adjuster, it would have been obvious for one of ordinary skill in the art to implement the same features taught by Lynn where the adding of the parameter to the eventual control signal takes place at the comparator which is buffered through the attack/decay timer generator (See Fig. 2, items 24, 30, and 32).

Regarding claim 5, Lynn teaches a gain determining stage according to claim 1 wherein the parameter is dependent on the peak value of the received signal (where the parameter is the comparator output pulse when the peaks of the input signal received through input 12 (Fig. 2) exceed the threshold; Lynn, Col. 2, line 54-56).

Regarding claim 6, Lynn teaches a gain determining stage according to claim 5 wherein the parameter is a peak level envelope signal (the attack/decay timing generator produces the analog control voltage which is an envelope signal of the comparator; Lynn, Col. 4, lines 20-24).

Regarding claim 7, Lynn teaches a gain determining stage according to claim 1 further comprising an input to receive a threshold signal; a comparator for comparing an

output of the adjuster with the threshold signal; and wherein the gain selector determines the gain dependent on the comparison (comparator inputs signal from threshold reset timer and compares it with the output (by way of the driver) of the variable gain amplifier an then the comparator sends the signal on to the variable gain amplifier; Lynn, Fig. 2, Col. 4, lines 17-19 and 27-31).

Regarding claim 8, Lynn teaches a gain determining stage according to claim 7 wherein the threshold signal is input to a processor before being passed to the comparator (the control voltage passes through the threshold/reset timer which processes the signal by switching it to a lower level through logarithmic conversion before passing to the comparator; Lynn, Col. 2, lines 58-62).

Claim 9 is rejected under 35 U.S.C. 103(a) for the same reasons as claim 3 because the two claims are identical to each other.

Regarding claim 11, Lynn teaches the gain determining stage of claim 7 wherein the gain is determined using a variable gain function: (a) when the output of the adjuster is greater than the threshold signal and a negative signal polarity; or (b) when the output of the adjuster is less than the threshold signal and a positive signal polarity is utilized (when the output signal has not exceeded the compression threshold, the control voltage determines the gain; Lynn, Col. 4, lines 48-51).

Regarding claim 12, Lynn teaches the gain determining stage of claim 11 wherein the variable gain function, or a factor of the variable gain, is: $K = 2^{lgK}$ where $lgK = lgGs + m(lgGV + lgTA)$ where K is the gain, $lgGs$ is the volume control signal, $lgGV$ is the output of the adjuster, $lgTA$ is the threshold signal and m is a value indicative of a

predetermined operational characteristic curve. (There is only one possible real value for K in the equation: $K = 2^{lgK}$. K must be "1", so therefore lgK must be zero. Although not explicitly stated, Lynn inherently teaches that the control voltage will equal the product of the pre determined gain level (Col. 4, lines 7-10) with the sum of the variable amplifier output and the threshold voltage when the variable amplifier output turns to zero because then in that moment the control voltages equals the predetermined gain multiplied by the threshold voltage because the signal passing through to the attack/delay timer would be that of the lower threshold value; Lynn, Col. 3, lines 66-68).

Regarding claim 13, Lynn teaches a signal processing circuit for amplifying a digital audio signal, comprising: parameter determining processor for determining a parameter of said signal (comparator that determines when peaks of the input signal exceed the threshold; Lynn, Col. 2, line 54-56); a gain determining stage according to claim 1; and amplifier for amplifying said signal according to said gain signal (driver 18 (Fig. 2); Lynn, claim 5- part b).

Regarding claim 14, Lynn teaches a circuit according to claim 13 wherein the parameter determining processor is a peak detector (peak detecting comparator; Lynn, claim 5- part c).

Regarding claim 15, Lynn teaches a circuit according to claim 14 wherein the peak detector output is dependent on the peak levels in the signal waveform and time dependent decay characteristics, wherein the decay characteristic is further dependent on the frequency of said signal (if the threshold timer detects that the level of the power-boosted output exceeds the threshold of the comparator for a pre selected time (i.e. a

low frequency signal that changes less frequently), then the compression threshold of the comparator is switched to a lower level. The comparator threshold remains low until the continuous signal is removed. (i.e. the signal level drops because of alternating current sinusoids or similar waves that characterize audio/voice signals); Lynn, Col.2, lines 58-64).

Regarding claim 16, Lynn teaches a circuit according to claim 15 wherein the peak detector comprises a disabler for disabling the decay characteristic until the signal changes polarity (if the lower threshold level (Col. 4, lines 56-59) is zero, the decay characteristic is disabled when the signal changes polarity).

Regarding claim 17, Lynn teaches a circuit according to claim 13 further comprising a delay for delaying said signal prior to said amplification in order to first determine said gain characteristic (delay for speech signal to determine gain without going into low compression; Lynn, Col. 3, lines 57-61).

Regarding claim 18, Lynn teaches a circuit according to claim 14 comprising: an input for receiving a signal (input 12; Lynn, Fig. 2); peak level processor for determining peak levels in the signal (peak detecting comparator; Lynn, claim 5- part c); and an output for outputting a signal dependent on said peak levels and a time dependent decay characteristic, wherein the decay characteristic is further dependent on the frequency of said received signal (if the threshold timer detects that the level of the power-boosted output exceeds the threshold of the comparator for a pre selected time (i.e. a low frequency signal that changes less frequently), then the compression threshold of the comparator is switched to a lower level. The comparator threshold

remains low until the continuous signal is removed. (i.e. the signal level drops because of alternating current sinusoids or similar waves of varying frequencies that characterize audio/voice signals); Lynn, Col.2, lines 58-64).

Regarding claim 19, Lynn teaches a detector according to claim 18 wherein the output comprises a disabler for disabling the decay characteristic until the signal changes polarity (if the lower threshold level {Col. 4, lines 56-59} is zero, the decay characteristic is disabled when the signal changes polarity).

Regarding claim 20, Lynn teaches a circuit according to claim 14 comprising: an input to receive an input audio signal (input 12; Lynn, Fig. 2); an amplitude processor operable in a decay mode, being when the input audio signal is smaller than a previous output signal, whereby in the decay mode, the processor is configured to generate a signal for decreasing the amplitude of a signal to be output (attack/decay timer; Lynn, Col. 2, 49-52); and a logic device for controlling the operation of the amplitude processor in the decay mode such that the processor only generates a signal in the decay mode upon receipt of a trigger from the logic device (the comparator triggers the attack/decay timing generator; Lynn, Col. 2, 49-52), whereby the trigger is related to the frequency of the input audio signal (trigger is related to the frequency of the audio signal because if the threshold timer detects that the level of the power-boosted output exceeds the threshold of the comparator for a pre selected time (i.e. a low frequency signal that changes less frequently), then the compression threshold of the comparator is switched to a lower level. The comparator threshold remains low until the continuous signal is removed. (i.e. the signal level drops because of alternating current sinusoids or

similar waves of varying frequencies that characterize audio/voice signals); Lynn, Col.2, lines 58-64).

Regarding claim 21, Lynn teaches a circuit according to claim 14 comprising: an input to receive in input audio signal (input 12; Lynn, Fig. 2); an amplitude processor configured to generate a signal for scaling the amplitude of a signal to be output (attack/decay timer which scales the control voltage which determines the amplitude of the output signal; Lynn, Col. 2, 49-52); and a logic device for controlling the operation of the amplitude processor such that the processor only generates the signal for scaling upon receipt of a trigger from the logic device (comparator triggers attack/delay timer; Lynn, Col. 2, 49-52), whereby the trigger is related to the frequency of the input audio signal (trigger is related to the frequency of the audio signal because if the threshold timer detects that the level of the power-boosted output exceeds the threshold of the comparator for a pre selected time (i.e. a low frequency signal that changes less frequently), then the compression threshold of the comparator is switched to a lower level. The comparator threshold remains low until the continuous signal is removed. (i.e. the signal level drops because of alternating current sinusoids or similar waves of varying frequencies that characterize audio/voice signals); Lynn, Col.2, lines 58-64).

Regarding claim 22, Lynn teaches the signal level detector of claim 20, further comprising a comparator for determining when a change for sign occurs (comparator, Lynn, Col.2, lines 58-64), wherein the comparator is associated with the logic device (comparator is the logic device, Lynn, Col.2, lines 58-64), and the logic device sends a trigger to the amplitude processor when a change of sign of the input signal occurs

(comparator sends trigger when signal hits threshold when threshold is at the point of a polarity change, Lynn, Col.2, lines 58-64).

Regarding claim 23, Lynn teaches the signal level detector of claim 20, wherein the logic device comprises an input for receiving a timeout signal (the comparator receives a timeout signal from threshold reset timer when the output exceeds the threshold of the comparator for a pre selected time; Lynn, Col. 2, lines 56-62), and the logic device sends a trigger to the processor when a timeout signal is received (the threshold of the comparator is switched to a lower level; Lynn, Col. 2, lines 58-62).

Regarding claim 24, Lynn teaches the signal level detector of claim 23, further comprising a timeout counter which is configured to generate the timeout signal after a time period passes, corresponding to the lowest frequency of the input signal, without a change of sign occurring (if the signal has not sufficiently changed and is continuous {i.e. a low-frequency signal}, the threshold reset timer will reset; Lynn, Col. 4, lines 37-45).

Regarding claim 39, Lynn teaches a method of amplifying a digital audio signal, comprising: determining a parameter of said signal (where the parameter is the peaks of the input signal sent through comparator to determine whether they exceed the threshold; Lynn, Col. 2, line 54-56); determining a gain signal according to claim 24; and amplifying said digital audio signal by applying said gain signal (variable gain amplifier which is controlled by control voltage; Lynn, Col. 2, lines 49-52).

Regarding claim 34, Lynn teaches the circuit of claim 21, further comprising a comparator for determining when a change for sign occurs (comparator, Lynn, Col.2,

lines 58-64), wherein the comparator is associated with the logic device (comparator is the logic device, Lynn, Col.2, lines 58-64), and the logic device sends a trigger to the amplitude processor when a change of sign of the input signal occurs (comparator sends trigger when signal hits threshold when threshold is at the point of a polarity change, Lynn, Col.2, lines 58-64).

Regarding claim 35, Lynn teaches the circuit of claim 21, wherein the logic device comprises an input for receiving a timeout signal (the comparator receives a timeout signal from threshold reset timer when the output exceeds the threshold of the comparator for a pre selected time; Lynn, Col. 2, lines 56-62), and the logic device sends a trigger to the processor when a timeout signal is received (the threshold of the comparator is switched to a lower level; Lynn, Col. 2, lines 58-62).

Regarding claim 36, Lynn teaches the signal level detector of claim 35, further comprising a timeout counter which is configured to generate the timeout signal after a time period passes, corresponding to the lowest frequency of the input signal, without a change of sign occurring (if the signal has not sufficiently changed and is continuous {i.e. a low-frequency signal}, the threshold reset timer will reset; Lynn, Col. 4, lines 37-45).

Regarding claim 29, Lynn suggests an integrated circuit comprising a circuit stage according to claim 13 (a peak detector is employed to aid in circuit integration; Lynn, Col. 2, lines 24-25). Although Lynn does not explicitly disclose that the signal processing circuit of claim 13 is embodied in an integrated circuit, Lynn does teach that one of the features of the invention, a peak detector, aids in circuit integration implying

that the intended embodiment of the invention is in an integrated circuit. Therefore it would have been obvious for one of ordinary skill in the art to implement the signal processing circuit of claim 13 as an integrated circuit based on the disclosed motivation of Lynn to create features (i.e. peak detector) that aid in integration of the circuit.

Regarding claim 30, Lynn teaches audio equipment comprising an integrated circuit according to claim 29 (voice signal compression system; Lynn, Col. 2, lines 39-41).

Regarding claim 37, Lynn teaches a method of determining a gain signal for applying to a digital audio signal (voice signal compression system including variable gain amplifier for amplifying the voice input signal; Lynn, Col. 2, lines 39-43); the method comprising: receiving a parameter of said digital audio signal (where the parameter is the comparator output pulse indicating when the peaks of the input signal exceed the threshold; Lynn, Col. 2, line 54-56); adjusting said parameter dependent on a received volume control signal (where the adjuster is the variable gain amplifier which is controlled by control voltage; Lynn, Col. 2, lines 49-52); applying a variable gain function to said volume control signal in order to generate the gain signal for applying to the digital audio signal (where the gain selector is the variable gain amplifier which is controlled by control voltage; Lynn, Col. 2, lines 49-52), and wherein said variable gain function is dependent on said adjusting parameter (control voltage which is produced by attack/delay timing generator dependent on the peaks of the input signal; Lynn, Col. 2, lines 49-56).

Regarding claim 38, Lynn teaches the method of claim 37 wherein the parameter is the peak level envelope signal of the digital audio signal (the attack/decay timing generator produces the analog control voltage which is an envelope signal of the comparator; Lynn, Col. 4, lines 20-24).

Regarding claim 25, Lynn teaches a method according to claim 38 wherein determining the peak level envelope comprises receiving an input audio signal (input 12; Lynn, Fig. 2); comparing the input audio signal with a previous output signal to obtain a difference signal (means for comparing the power-boosted output signal and an initial threshold signal to provide a comparator output corresponding to the difference between the power-boosted output signal and the initial threshold signal; Lynn, claim 1-b); generating a scaled signal by scaling the difference signal using an attack coefficient or a decay coefficient (attack/decay timer which scales the control voltage which determines the amplitude of the output signal; Lynn, Col. 2, 49-52), depending upon the comparison; combining the scaled signal with the previous output signal to obtain a signal, indicative of the signal level of the input audio signal, characterized in that the method comprises: controlling the generation of the scaled signal when scaled by the decay parameter, using a trigger related to the frequency of the input audio signal (trigger is related to the frequency of the audio signal because if the threshold timer detects that the level of the power-boosted output exceeds the threshold of the comparator for a pre selected time (i.e. a low frequency signal that changes less frequently), then the compression threshold of the comparator is switched to a lower level. The comparator threshold remains low until the continuous signal is removed. (i.e.

the signal level drops because of alternating current sinusoids or similar waves of varying frequencies that characterize audio/voice signals); Lynn, Col.2, lines 58-64).

Regarding claim 26, Lynn teaches the method of claim 25 wherein only the generation of the indicative signal scaled signal by a decay parameter is controlled (attack/decay timer which scales the control voltage which determines the amplitude of the output signal; Lynn, Col. 2, 49-52).

Regarding claim 27, Lynn teaches the method of claim 25, wherein the trigger is generated when a change of sign of the input signal occurs or a timeout occurs (the comparator receives a timeout signal from threshold reset timer when the output exceeds the threshold of the comparator for a pre selected time and the threshold of the comparator is switched to a lower level; Lynn, Col. 2, lines 56-62).

Regarding claim 32, where there is processor control code to, when, running, implement the signal processing method of claim 37, Lynn doesn't teach a code or computer program of running the method of gain determination as in claim 37 as required, although it would have been obvious for one of ordinary skill in the art to do so because taking a process and making it automatic through programming or coding without any unexpected result requires only routine skill in the art.

Regarding claim 33, although Lynn does not explicitly teach a carrier carrying the processor control code of claim 32, it would have been obvious for one of ordinary skill in the art to use a carrier where carrier refers to a carrier signal (as in modulation) or when carrier refers to a communications company infrastructure that supports telephone or internet transmissions because using either of these involves routine skill in the art.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Larsen et al. (US Pat. No. 5,303,308) teaches a compression system for an audio device which will apply a gain to an input signal based on frequency properties of the signal. Frindle (US Pub. No. 2002/0173865) teaches a digital audio signal processing system utilizing compression and a peak level detector.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to KILE O. BLAIR whose telephone number is (571)270-3544. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Joe H. Cheng can be reached on (571) 272-4433. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

KB
11/26/07

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